MICROWAVE Si POWER TRANSISTOR WITH MONOLITHICALLY FABRICATED IMPEDANCE MATCHING CIRCUITS

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Abstract

A new technology is demonstrated for microwave Si power transistor manufacturing. Based on flip-chip technology and M/A-COM's glass based technology, impedance matching circuits in microwave Si power transistor can be fabricated monolithically using standard thin film processes. Thus the high manufacturing cost for microwave Si power transistors, primarily associated with the package and assembly, can be substantially reduced. 1.88 Ghz Si power transistors were fabricated using the new technology. In CW common emitter operation mode, 5W of output power is obtained with 11dB of gain and 39% of power added efficiency, at Vcc=25V and Icq=25mA.

I. Introduction.

Due to the explosive development in wireless communication industry, the demand on microwave power amplification is increasing dramatically. Up to now, most of the base station amplifiers use Si bipolar junction transistors (BJT) as their main power amplification devices. Although the Si device fabrication technology is mature, the Si high power device packaging technology is still based on the technology developed many years ago. For high power microwave applications the Si power transistor package requires: 1) internal impedance matching circuits[1] and 2) a very high thermal conduction path. In order to deliver a large amount of power, Si devices typically have very large emitter periphery, hence very low input and output impedance's. Thus internal impedance matching circuits are required for all Si power transistors. Due to its conductive nature Si substrate is not suitable for low loss RF circuits[2]. Hence the impedance matching circuits can not be fabricated onto Si substrates. On the other hand these Si power devices have to dissipate large amount of heat, therefore a ceramic BeO substrate has to be used to achieve low thermal resistance. Because of its surface roughness the ceramic BeO substrate can not support thin film processes. Thus, up to now, the internal impedance matching circuits can only be realized using chip capacitors and bonding wires. Fig.1 shows the inside of a typical packaged microwave Si power transistor. As shown in Fig.1 all the inductors in the impedance matching circuits are formed by bonding wires. Since the inductance values are very critical, the length and shape of these wires have to be tightly controlled. It is common to

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manually tune the impedance matching circuits by reshaping the bonding wires. Although this technology is being used throughout the Si power transistor industry, it is, by its nature, a complex and labor intensive technology.

In this study a new technology for microwave Si power transistor manufacturing is demonstrated. In this new technology the internal impedance matching circuits are fabricated monolithically onto a low loss glass based substrate, then a Si device and impedance matching circuits are seamless integrated together. Thus the new technology will eliminate all the chip capacitors and bonding wires replacing them with monolithically printed inductors and thin film capacitors. Being completely different from the existing technology, this new technology will not only reduce the manufacturing and package cost, but also improve the device performance and reliability. This technology was initially demonstrated on pulsed Si power transistors[3]. By further improving the thermal characteristics of the package this technology is also proven suitable for CW operated Si power transistors. At 1.88 Ghz and in common emitter CW operation, 5W of output power is obtained with 11dB of gain and 39% of power added efficiency, at Vcc=25V and Icq=25mA. This transistor basically forms a building block, and transistors for higher output power can be obtained simply by paralleling these transistors together with minor modifications to input and output circuits.

II. Description

Basically the new technology utilizes the glass based technology for impedance matching circuit fabrication and flip-chip technology for integrating the Si power transistor into the substrate. Fig. 2 shows a conceptual drawing for the new microwave Si power transistor package.

The glass based technology, developed at M/A-COM, combines the properties of Si and glass to create a low loss substrate for microwave circuits. As shown in Fig. 2, the basic substrate consists of Si pedestals embedded in a glass medium. The Si pedestals provide both electrical grounding and a thermal conduction path while the glass provides electrical isolation and mechanical support. Since glass can be polished to a fine surface finish, it readily supports the thin film process. Hence all the passive elements required for impedance matching circuits now can be fabricated using monolithic processes. The detailed process has been reported previously [3, 4].

The flip-chip technology , also developed at M/A-COM, accommodates both electrical and thermal requirements for Si microwave power transistor package. The bump metal consists of Au/Pt/Au:Sn multilayer structure. Au is chosen to form the major portion of the bump due to its high electric and thermal conductivity's. The bump is designed to cover the entire active area on the Si device to maximize the thermal conduction path. The bond between the Si device and the substrate is formed by reflowing the Au:Sn layer. The reflow is carried out in formic acid vapor to insure a good, void-free contact.

This technology worked well for pulse operated Si power transistors[3]. In order to meet the thermal requirements for CW operation further improvement is needed. It was found that the dielectric passivation layer on the Si device has detrimental effect on the thermal characteristic of the package. As shown in Fig. 2 the Si device is flip-chip mounted onto the substrate, therefore the dielectric passivation layer is in the thermal conduction path. Due to its amorphous nature, this layer has very low thermal conductivity. So it is obvious that minimizing the thickness of this passivation layer will further reduce the thermal resistance of the package.

This new technology was demonstrated on an 1.88 Ghz Si power transistor. The transistor was designed for CW class AB operation in common emitter configuration. The impedance matching circuits were designed using HP Microwave-Design-System (MDS) and implemented onto the glass based substrate. The passive elements, both inductors and capacitors, were fabricated using a

standard thin film batch processes. The Au/Pt/Au:Sn multilayer bump was fabricated on the Si device using metal evaporation/lift-off processes. To minimize the thermal resistance, the thickness of the passivation dielectric layer was reduced to 15% of its original thickness. The base and emitter contacts were formed by flip-chip bonding and the collector contact, which is on the backside of the device, was formed by wire bonds.

III. Results and Discussions

The finished microwave Si power transistors were DC and RF tested. The glass based substrate with mounted Si power transistor was mounted into a ceramic package using Au:Sn preform. Fig. 3 showed a packaged device in a testing fixture. For RF power testing the package was fully characterized by an HP 8510 before being connected into a Maury Automatic Load-pull system which was calibrated at 1.88 GHz. The device was biased at 25V and the quiescent current was set to be 25mA. A low pass filter was used between the tuner and the power detector to filter out the harmonic components from the device. Fig.4 shows the power contours of the device. The optimum source was at (-0.62, -0.46) which was transformed from virtually short by the input impedance matching circuit. The optimum load was at (-0.30, 0.20) due to the output impedance matching circuit. The total circuit size is 3mmx2mm. Fig. 5 depicts the power saturation characteristics of the finished power transistor. Without any tuning the device delivered 5W power with 11dB of gain and 39% of power added efficiency. Because of the flip-chip mounting configuration the backside of the Si device is now mechanically accessible. It is possible that an additional thermal conduction path can be formed which will further reduce the package thermal resistance. Therefore, this new technology will not only eliminate all the chip capacitors and most bonding wires but also create new ways to further improve the Si power transistor package which will have profound impact on the future Si power transistor package technology.

IV. Conclusion

A new Si power transistor manufacturing technology is demonstrated and it is shown that the new technology will not only substantially simplify the Si power transistor assembly and packaging but also provide new ways to further improve the Si power transistor package.

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References

[1] Richard Allison, " Silicon bipolar microwave power transistors", IEEE Trans, Microwave Theory Tech., Vol. MTT-27, pp415-422,1979.
[2] T. M. Hyltin, "Microstrip transmission line on semiconductor substrates", IEEE Trans, Microwave Theory Tech., Vol. MTT-13, pp777-781, 1965.
[3] Ping Li, Timothy Boles, "A new technology for Si microwave power transistor manufacturing", 1995 IEEE MTT-S Digest, pp103-106, 1995.
[4] P. Chinoy, et al, "Manufacture of low-loss microwave circuits using HMIC technology", 1994 IEEE MTT-S Digest, pp1137-1140, 1994.

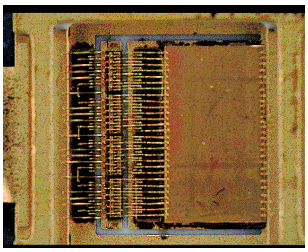

Fig. 1. A Si power transistor with internal matching circuits made using the existing technology

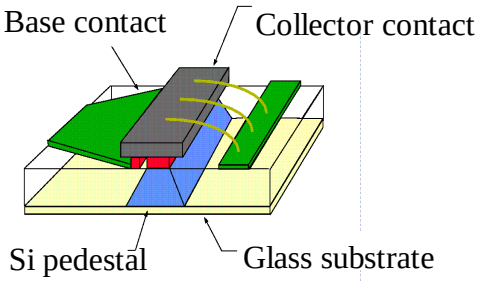

Fig. 2 A conceptual drawing of the new package for microwave Si power transistors.

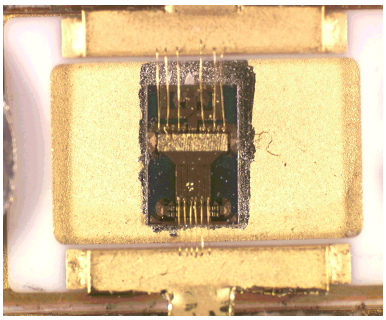

Fig. 3a The close view of the packaged Si power transistor fabricated using new technology.

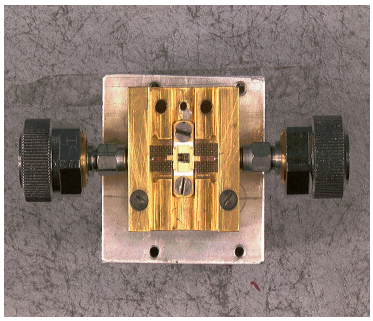

Fig. 3b The packaged Si power transistor in a testing fixture.

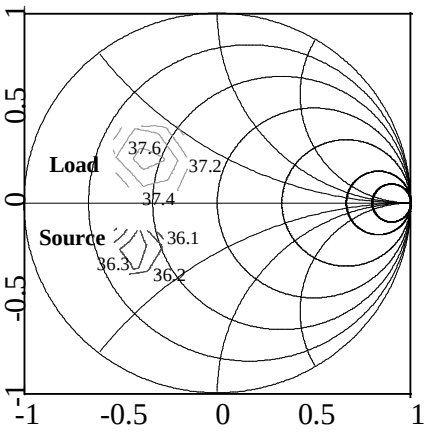

Fig.4 The power contour for flip-chip mounted Si power transistor with input and output impedance matching circuits. Vcc=25V, Icq=25mA,Freq=1.88GHz.

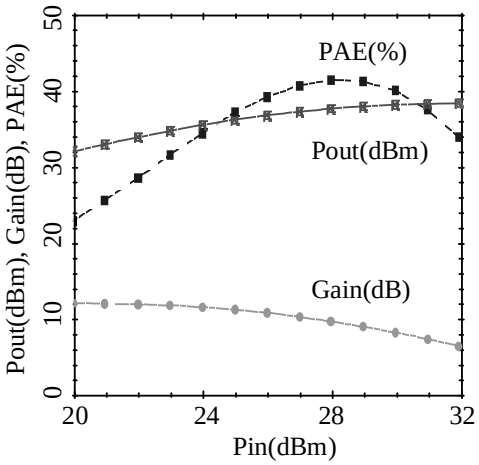

Fig.5 The power saturation characteristic of the packaged Si microwave power transistor. Vcc=25V, Icq=25mA, Freq=1.88GHz.

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